TDA9950

CEC/I²C-bus translator

Rev. 02 — 22 October 2009 Product data sheet

1. General description

The TDA9950 is a single-chip CEC/I²C-bus translator with a processor, dedicated to the control and interfacing of the Consumer Electronics Control (CEC), a feature of the High-Definition Multimedia Interface (HDMI).

The TDA9950 is an interface between the CEC protocol and timings and the standard I²C-bus. A message received on the I²C-bus interface is written in a buffer and sent on the CEC line. A message received from the CEC line is stored in a buffer, and an interrupt is generated indicating that a message can be read via the I²C-bus. To reduce its power consumption the TDA9950 sets itself to Idle mode when there is no message on the CEC line nor on the I²C-bus.

2. Features

2.1 Principal features

- Receive and transmit CEC messages with compliant Signal Free Time handling
- I²C-bus interface to host supporting 100 kbit/s and 400 kbit/s communication
- Supports multiple CEC logical addresses
- Supports CEC messages up to 16 bytes in length
- Programmable retry count
- Comprehensive arbitration and collision handling
- 3.0 V to 3.6 V V_{DD} operating range
- Automatic Idle mode to reduce power consumption when there is no message on CEC line and I²C-bus
- I/O pins are 5 V tolerant

2.2 Additional features

- Processor with embedded software to control the interface between CEC line and I²C-bus
- Active-LOW reset input and on-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets.
- On-chip oscillator for 12 MHz crystal
- Schmitt trigger port inputs

founded by Philips

3. Applications

- All devices using an HDMI connector
- YC_BC_R or RGB high-speed video digitizer
- Projector, plasma and LCD TV
- Rear-projection TV
- High-end TV
- Home-theater amplifier
- DVD recorder

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
T_{amb}	ambient temperature		0	-	70	°C
P_{tot}	total power dissipation	Operating mode	-	33	46.8	mW
		Idle mode	-	16	25.2	mW
I²C-bus: (5 V tolerant) pins SDA and SCL						
f_{clk}	clock frequency	Standard mode	-	-	100	kHz
		Fast mode	-	-	400	kHz

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9950TT	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

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6. Block diagram

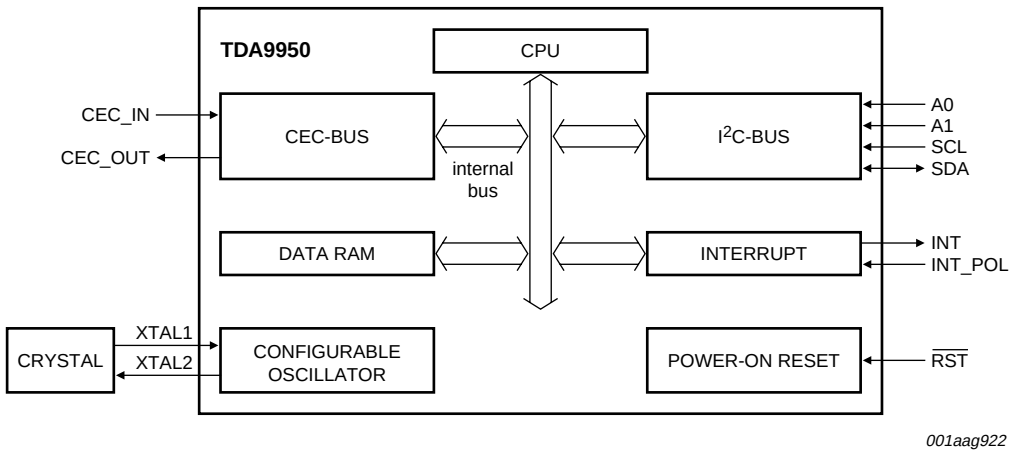


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

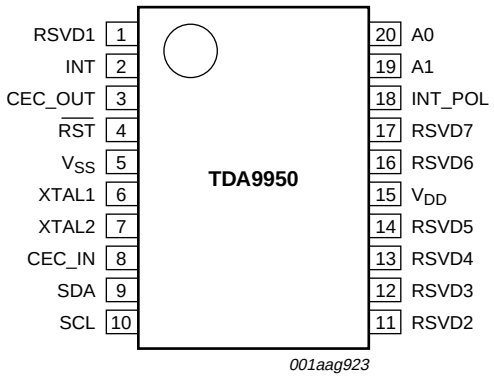


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
RSVD1	1	I	**RSVD1 —** Reserved pin; shall be connected to ground
INT	2	O	**INT —** Interrupt line to the host processor to indicate data is available for reading. The polarity of this signal depends on the state of pin INT_POL.
CEC_OUT	3	O	**CEC_OUT —** Output for CEC line (open-drain).

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Table 3. Pin description *…continued*

Symbol	Pin	Type[1]	Description
$\overline{RST}$	4	I	**$\overline{RST}$ —** External reset input. A LOW state on this pin resets the translator.
V_{SS}	5	P	**Ground:** 0 V reference (GND).
XTAL1	6	I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (12 MHz crystal).
XTAL2	7	O	**XTAL2 —** Output from the oscillator amplifier.
CEC_IN	8	I	**CEC_IN —** Input for CEC line.
SDA	9	I/O	**SDA —** I²C-bus serial data input/output (open-drain).
SCL	10	I	**SCL —** I²C-bus serial clock input.
RSVD2	11	I	**RSVD2 —** Reserved pin (should be connected to ground).
RSVD3	12	O	**RSVD3 —** Reserved pin.
RSVD4	13	O	**RSVD4 —** Reserved pin.
RSVD5	14	I	**RSVD5 —** Reserved pin (should be connected to ground).
V_{DD}	15	P	**Power supply —** This is the (core digital 3.3 V) power supply voltage for normal operation as well as Idle and Power-down modes.
RSVD6	16	I	**RSVD6 —** Reserved pin (should be connected to ground).
RSVD7	17	I	**RSVD7 —** Reserved pin (should be connected to ground).
INT_POL	18	I	**INT_POL —** Sets the polarity of the active output required on the INT signal (pin 2). Leave floating or pull-up to V_{DD} for a HIGH output when active (rising edge), connect to V_{SS} for a LOW output when active (falling edge). This input is latched at reset.
A1	19	I	**A1 —** I²C-bus slave address bit 2.
A0	20	I	**A0 —** I²C-bus slave address bit 1.

[1] I = input, O = output, P = power supply.

8. Functional description

The TDA9950 uses an internal processor with embedded software to control the interface between the CEC line and the I²C-bus.

8.1 Device addressing

The TDA9950 is a slave I²C-bus device and the SCL pin is an input pin only. The timing and protocol for the I²C-bus are standard.

Table 4. Device address code

Address code	Device code					Chip enable		R/$\overline{W}$
Bit	b7[1]	b6	b5	b4	b3	b2	b1	b0
Value	0	1	1	0	1	A1	A0	R/$\overline{W}$

[1] The Most Significant Bit (MSB), b7, is sent first.

A1 and A0 are hardware-selectable pins.

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In case of independent CEC, a system could have up to four TDA9950 devices on the same I²C-bus.

The four addresses are defined by the state of the inputs A0 and A1 (logic 1 when connected to V_{DD}, logic 0 when connected to GND).

8.2 Configuring the TDA9950

The TDA9950 is controlled via a series of registers.

Table 5. I²C-bus register configuration

Register	Description	Address	Read/Write
APR	Address Pointer Register	00h	W
CSR	TDA9950 Status Register	00h	R
CER	TDA9950 Error Register	01h	R
CVR	TDA9950 Version Register	02h	R
CCR	TDA9950 Control Register	03h	R/W
ACKH	CEC Address ACK High register	04h	R/W
ACKL	CEC Address ACK Low register	05h	R/W
CCONR	CEC Configuration Register	06h	R/W
CDR	CEC Data Registers	07h - 19h	R/W

The first byte of any I²C-bus write frame configures the address pointer register APR, which determines the first TDA9950 register that will be read or written in the remainder of the I²C-bus transfer. If a read is carried out without a prior write to the address pointer register, the register returned will be that to which the address pointer register was last set.

The address pointer auto-increments after a successful read or write for all address pointer values other than 00h. Auto-incremented addresses above 19h are invalid and ignored.

Registers 01h to 06h are used for configuration of the TDA9950, whilst repeated auto-incremented reads starting at register 07h are used to transfer CEC data. Setting the address pointer register higher than 07h is treated as setting it to 07h, as all message data transfers must start from register 07h and continue by auto-incrementing in one contiguous transfer. Transfers via the data registers are formatted using the data register protocol described in Section 8.5.

8.3 Use of the INT line

As the TDA9950 is an I²C-bus slave device, it provides an additional I/O line to signal to the host that data is available for reading. This is the INT output line, which should be monitored by the host. An additional TDA9950 input, on pin INT_POL, allows configuration of the polarity of operation of the INT line. When the INT line is active, it will match the state of the input on pin INT_POL.

The state of the INT line is always reflected in the TDA9950 Status Register, so it is possible to regularly poll this register instead of monitoring the INT line. However, this method is less efficient and not recommended. The INT indication in the TDA9950 Status Register is not affected by the setting of the INT polarity input on pin INT_POL.

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8.4 Register descriptions

Table 6. APR - Address Pointer Register (address 00h) bit description (Write mode)

Bit	Symbol	Description
7 to 5	reserved	reserved (must be set to 000)
4 to 0	REG_PTR[4:0]	**Address Pointer:** Address of the register that will be read/written during further I²C-bus communication.

Table 7. CSR - TDA9950 Status Register (address 00h) bit description (Read mode)

Bit	Symbol	Description
7	BUSY	**BUSY:** 0 = the TDA9950 is able to handle requests. 1 = the TDA9950 is busy and cannot accept any further request.
6	INT	**INT:** 0 = the INT interrupt output is inactive. 1 = the INT interrupt output is active.
5	ERR	**ERR:** 0 = no error. 1 = an error occurred (specified in the TDA9950 Error Register). Cleared by a read of the TDA9950 Error Register.
4 to 0	-	not used

Table 8. CER - TDA9950 Error Register (address 01h) bit description (Read only)

Bit	Symbol	Description
7 to 0	CER[7:0]	**TDA9950 Error Register:** This register provides details of the last error that occurred. Reading this register resets the ERR bit in the TDA9950 Status Register. 00h = no error has occurred since reset. 01h = watchdog reset has occurred. 02h = long CEC message with no End Of Message (EOM) detected. 03h = CEC overrun - no buffer available to receive.

Table 9. CVR - TDA9950 Version Register (address 02h) bit description (Read only)

Bit	Symbol	Description
7 to 4	CVR_MAJ[3:0]	**TDA9950 major version register:** Major version
3 to 0	CVR_MIN[3:0]	**TDA9950 minor version register:** Minor version

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Table 10. CCR - TDA9950 Control Register (address 03h) bit description (Read/Write)

Bit	Symbol	Description
7	RESET	**RESET:** Resets the TDA9950. Any transmission in progress will be completed first - the reset occurs once the TDA9950 returns to the idle state. All default values will be restored. 0 = no specific action. 1 = resets the TDA9950.
6	ON_OFF	**ON_OFF:** 0 = the TDA9950 is disabled (after completion of any pending CEC transmission or reception) and will no longer acknowledge any message on the CEC line or accept any message for transmission. 1 = the TDA9950 is enabled and will acknowledge messages according to the logical address bits in the CEC Address ACK High and CEC Address ACK Low registers.
5 to 0	-	not used

Table 11. ACKH - CEC Address ACK High register (address 04h) bit description (Read/Write)

Bit	Symbol	Description
7	reserved	reserved (must be set to 0)
6 to 0	ACKH[6:0]	**CEC Address ACK High register** For each bit: 0 = messages to the corresponding logical address will not be acknowledged. 1 = messages to the corresponding logical address are acknowledged and forwarded to the host.

Table 12. ACKL - CEC Address ACK Low register (address 05h) bit description (Read/Write)

Bit	Symbol	Description
7 to 0	ACKL[7:0]	**CEC Address ACK Low register** For each bit: 0 = messages to the corresponding logical address will not be acknowledged. 1 = messages to the corresponding logical address are acknowledged and forwarded to the host.

Table 13. CCONR - CEC Configuration Register (address 06h) bit description (Read/Write)

Bit	Symbol	Description
7 to 5	-	not used

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Table 13. CCONR - CEC Configuration Register (address 06h) bit description (Read/Write)

Bit	Symbol	Description
4	ENABLE_ERROR	**ENABLE_ERROR:** 0 = no specific action. 1 = notify the host of all errors via the TDA9950 Error Register and via the CECData.err service (see Section 8.5.4).
3	-	not used
2 to 0	RETRY[2:0]	**RETRY[2:0]:** retry count to be used by the TDA9950. The maximum value is 5; values greater than 5 will still give 5 retries.

Table 14. CDR[0:18] - CEC Data Registers (addresses 07h to 19h) bit description (Read/Write)

Bit	Symbol	Description
7 to 0	FrameByteCount/ ServiceSelector/ Parameters[7:0]	**FrameByteCount/ServiceSelector/Parameters:** Length of message in B, Type of message, 17 B for message content; see Section 8.5 “Data register protocol”.

8.5 Data register protocol

Communication between the TDA9950 and the host using the CEC Data Registers is carried out using frames of information. The host is the master of all data transfers; the TDA9950 uses the INT line to inform the host that it has data available.

Before a frame is read or written, the host must set the REG_PTR field in the Address Pointer Register to the base CEC Data Register address. Successive reads or writes automatically increment the REG_PTR as the frame is transferred. Message transfers can only start from the first CEC Data Register at address 07h and not from higher addresses, as messages must be transferred complete and not in fragments.

Each frame consists of a byte count, a service selector and then zero or more (up to 17) parameters as shown in Figure 3.

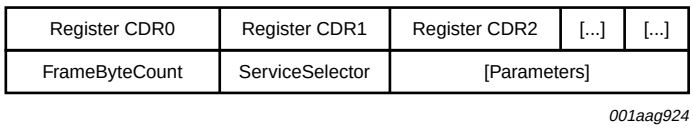


Fig 3. Frame format for the data register protocol

The FrameByteCount indicates the number of bytes in the frame (including the FrameByteCount itself). The service is specified by the ServiceSelector (see Table 15). The remaining bytes of the frame, if any, contain the parameters associated with a particular service. The maximum length of a frame is 19 bytes. The TDA9950 will only accept a single outstanding request. Reading message bytes beyond FrameByteCount will return FFh.

Table 15 shows the organization of the ServiceSelector values. If an unused ServiceSelector is sent to the TDA9950 it will respond with the confirmation Bad .req service (see Table 17). For every service, the parameters that are defined in the following sections are mandatory. No service contains optional parameters.

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Table 15. CEC Data services

ServiceSelector	From host to TDA9950	From TDA9950 to host	Section
00h	CECData.req		8.5.1
01h		CECData.cnf	8.5.2
81h		CECData.ind (indication, no TDA9950 error)	8.5.3
82h		CECData.err (no indication, TDA9950 error)	8.5.4
83h		CECData.ier (indication, TDA9950 error)	8.5.5

8.5.1 CECData.req service

This service is used to transfer CEC message data. The parameters for the service are shown in Table 16. Transmission of the CEC message commences as soon as the complete message has been received by the TDA9950 (subject to the appropriate Signal Free Time rules being satisfied).

Table 16. Parameters for CECData.req service

Parameter	Comments
AddressByte	Source and destination logical addresses in the form SSSS DDDD
DataBytes	Bytes of message data up to the data length indicated by FrameByteCount

8.5.2 CECData.cnf service

This service is used by the TDA9950 to inform the host of the success or other result of a CECData.req service. The parameters are shown in Table 17.

Table 17. Parameters for CECData.cnf service

Parameter	Comments	Value	Meaning
ResultCode	A value indicating the result of the transmission	00h	Success
		80h	TDA9950 in off state
		81h	Bad .req service
		82h	Failed, unable to access CEC line
		83h	Failed, arbitration error
		84h	Failed, bit timing error
		85h	Failed, destination address not acknowledged
		86h	Failed, data byte not acknowledged

8.5.3 CECData.ind service

This service is used to transfer a CEC message, received from a remote device, to the host. The parameters are listed in Table 18.

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Table 18. Parameters for CECData.ind service

Parameter	Comments
AddressByte	Source and destination logical addresses in the form SSSS DDDD
DataBytes	Bytes of message data up to the data length indicated by FrameByteCount

8.5.4 CECData.err service

This service is used to alert the host to an error condition. There are no parameters. The host should read the TDA9950 Error Register CER for details of the error. This indication will only occur when bit ENABLE_ERROR of the CEC Configuration Register CCONR is set to enable error indications.

8.5.5 CECData.ier service

This service is used to transfer a CEC message, received from a remote device, to the host. In addition, it also alerts the host to an error condition. The parameters are listed in Table 19. The host should read the TDA9950 Error Register CER for details of the error. This indication will only occur when bit ENABLE_ERROR of the CEC Configuration Register CCONR is set to enable error indications.

This service will not be used if no such errors are implemented.

Table 19. Parameters for CECData.ier service

Parameter	Comments
AddressByte	Source and destination logical addresses in the form SSSS DDDD
DataBytes	Bytes of message data up to the data length indicated by FrameByteCount

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8.6 Example communication sequences

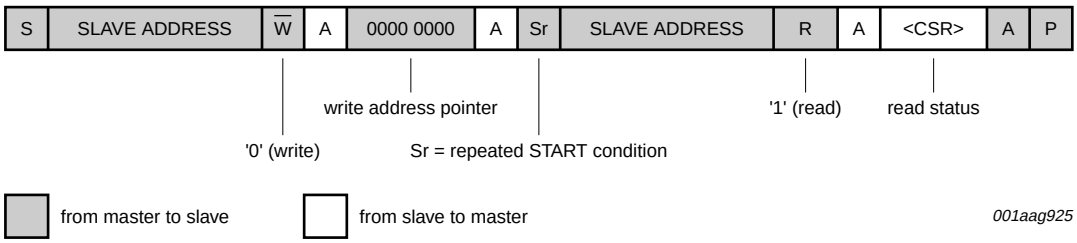
When writing, the first byte after the slave address will contain the Address Pointer Register value. Subsequent bytes are written to the register addressed by the Address Pointer Register.

If the host wishes to write to two or more discontiguous registers, two separate write sequences must be used with a STOP/START or repeated START condition between them. Contiguous ranges of registers can be written in one communication sequence between a START and STOP condition. Messages in the CEC Data Registers must be written and read as contiguous ranges of registers.

When reading, values are read starting at the register currently addressed by the Address Pointer Register. The pointer auto-increments after each read. If the host should read past register 19h, or read more bytes than indicated by the FrameByteCount in register CDR[0] (address 07h), the value FFh will be returned.

When the address pointer is 00h, it does not auto-increment. This allows repetitive polling of the TDA9950 Status Register without the need to reset the Address Pointer Register.

If the address pointer needs to be set before a read takes place, the host must first write to the Address Pointer Register and then, after a repeated start condition (or a STOP/START sequence), commence reading as many data bytes as it requires.

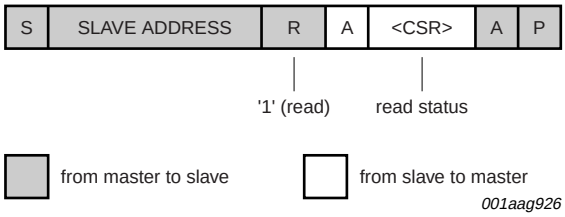


A = acknowledge (SDA = LOW)

S = START condition

P = STOP condition

Fig 4. Host reads TDA9950 Status Register - after setting address pointer



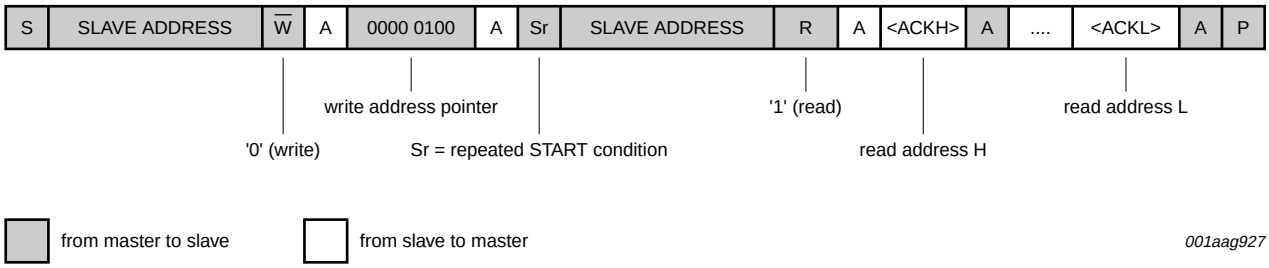
A = acknowledge (SDA = LOW)

S = START condition

P = STOP condition

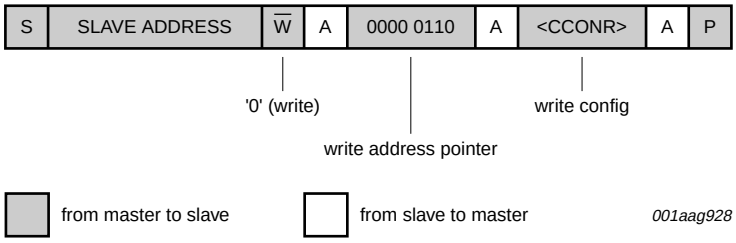
Fig 5. Host reads TDA9950 Status Register - without setting address pointer (was at 0)

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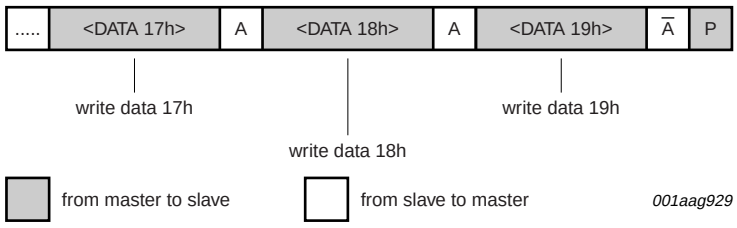
A = acknowledge (SDA = LOW)
S = START condition
P = STOP condition
R = read
$\overline{W}$ = write

Fig 6. Host reads CEC Address ACK registers - after setting address pointer



A = acknowledge (SDA = LOW)
S = START condition
P = STOP condition
$\overline{W}$ = write

Fig 7. Host writes CEC Configuration Register - after setting address pointer



A = acknowledge (SDA = LOW)
$\overline{A}$ = not acknowledge (SDA = HIGH)
P = STOP condition

Fig 8. Host writes last three CEC Data Registers

8.6.1 Notes on writing the CEC Data Registers

- The CEC Data Registers should be written starting from the first CEC Data Register, for the number of registers indicated by the contents of that first CEC Data Register, in one contiguous operation.

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- The length of the message is given by the byte in the first CEC Data Register. This will be at least 3 for the shortest message. A value less than 3 indicates an invalid message.
- If fewer CEC Data Registers are written than the number indicated by the first CEC Data Register, the partial message will be ignored and no confirmation will be returned.
- If more CEC Data Registers are written than the number indicated by the first CEC Data Register, the message will be processed as soon as the message's last CEC Data Register is written, and the extra bytes written will be ignored.
- If the highest CEC Data Register is written and more message bytes are indicated by the first CEC Data Register, the message will be processed as soon as the highest CEC Data Register is written, and the extra bytes written will be ignored.

8.6.2 Notes on reading the CEC Data Registers

- The CEC Data Registers only contain a valid message when the INT line is set and the INT bit in the TDA9950 Status Register is set.
- If CEC Data Registers are read when the INT line is not set, the first CEC Data Register will contain 0, indicating that there are no bytes to read. Any further reads before a STOP condition will return the value FFh.
- The CEC Data Registers should be read starting from the first CEC Data Register, for the number of registers indicated by that first CEC Data Register, in one contiguous operation.
- If the host writes CEC Data Registers and then begins reading without first resetting the Address Pointer Register, reading will automatically commence from the first CEC Data Register.
- If reading stops before all indicated CEC Data Registers are read, the TDA9950 will reset the INT line and the message is discarded by the TDA9950 and will not be available for reading again.
- If reading continues for more CEC Data Registers than are indicated by the first CEC Data Register, the value FFh will be read. The INT line is reset when the last valid CEC Data Register for the current message is read.

8.7 Using the TDA9950

8.7.1 Initialization

After a reset, first configure the TDA9950 with its logical address or addresses (as required):

- **I2C_WRITE: 04h, 00h, 08h**

  Set Address Pointer to 04h (ACKH), set ACKH to 00h, and set ACKL to 08h.

  The TDA9950 is now configured to acknowledge messages to the logical address 3 (Tuner 1 (see HDMI1.3a specification) or STB1 (see HDMI1.2a specification)).

Then set the TDA9950 to the ON state (mandatory):

- **I2C_WRITE: 03h, 40h**

  Set Address Pointer to 03h (CCR), set CCR to 40h.

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The TDA9950 is now enabled. Messages addressed to logical address Tuner 1 (see HDMI1.3a specification) or STB1 (see HDMI1.2a specification) will be acknowledged and forwarded to the host processor.

8.7.2 Sending a CEC message

Example: the host processor of Playback Device 1 (see HDMI1.3a specification) or DVD1 (see HDMI1.2a specification) wishes to send the message <TextView On> to TV:

- **I2C_WRITE: 00h; I2C_READ, I2C_READ, ...**

  Set Address Pointer to 00h (CSR), read TDA9950 Status Register - repeat read until TDA9950 is no longer busy (bit CSR[7] = 0).

- **I2C_WRITE: 07h, 04h, 00h, 40h, 0Dh**

  Set Address Pointer to 07h (CEC Data Register 1), write CEC Data Registers. FrameByteCount = 4, ServiceSelector = CECData.req, AddressByte = DVD/TV, DataByte = <TextView On>.

- **Wait for INT line to be asserted**

  When TDA9950 has a response, it will assert the INT line (the host could also poll bit CSR[6]).

- **I2C_WRITE: 07h; I2C_READ: 03h, 01h, 00h**

  Set Address Pointer to 07h (Data Register 1), read CEC Data Registers. FrameByteCount = 3, ServiceSelector = CECData.cnf, ResultCode = Success.

8.7.3 Receiving a CEC message

Example: TV sends the message <Give Physical Address> to Playback Device 1 (see HDMI1.3a specification) or DVD1 (see HDMI1.2a specification):

- **INT line is asserted**

  The TDA9950 at Playback Device 1 (see HDMI1.3a specification) or DVD1 (see HDMI1.2a specification) has acknowledged the message from TV and it is now available for reading by the Playback Device 1 (see HDMI1.3a specification) or DVD1 (see HDMI1.2a specification) host processor.

- **I2C_WRITE: 07h; I2C_READ: 04h, 81h, 04h, 83h**

  Set Address Pointer to 07h (Data Register 1), read CEC Data Registers. FrameByteCount = 4, ServiceSelector = CECData.ind, AddressByte = TV/DVD, DataByte = <Give Physical Address>.

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9. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	ambient temperature		0	70	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin	all I/O and output pins	-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	80	mA
V_{xtal}	crystal voltage	on pins XTAL1, XTAL2	-	V_{DD} + 0.5	V
V_n	voltage on any other pin	except pins XTAL1, XTAL2, V_{DD}	–0.5	+5.5	V

[1] Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

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10. Static characteristics

Table 21. Static characteristics

V_{DD} = 3.0 V to 3.6 V; T_{amb} = 0 °C to +70 °C for industrial application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage			3.0	3.3	3.6	V
I_{DD}	supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz					
		Operating mode		-	10	13	mA
		Idle mode		-	5	7	mA
dV/dt	rate of change of voltage	rise rate of V_{DD}		-	-	2	mV/µs
		fall rate of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.2	V
$V_{th(HL)}$	negative-going threshold voltage	except pins SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	positive-going threshold voltage	except pins SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage	pins $\overline{RST}$, CEC_IN, SDA, SCL, RSVD2		-	$0.2V_{DD}$	-	V
V_{IL}	LOW-level input voltage	pins SCL, SDA only		–0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	pins SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{OL}	LOW-level output voltage	V_{DD} = 2.4 V to 3.6 V; pin CEC_OUT					
		I_{OL} = 20 mA	[2]	-	0.6	1.0	V
		I_{OL} = 3.2 mA	[2]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	V_{DD} = 2.4 V to 3.6 V; pin CEC_OUT					
		I_{OH} = –3.2 mA		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = –20 µA		V_{DD} – 0.3	V_{DD} – 0.2	-	V
V_{xtal}	crystal voltage	on pins XTAL1, XTAL2; with respect to V_{SS}		–0.5	-	+4.0	V
V_n	voltage on any other pin	except pins XTAL1, XTAL2, V_{DD}; with respect to V_{SS}		–0.5	-	+5.5	V
$V_{trip(bo)}$	brownout trip voltage	2.4 V < V_{DD} < 3.6 V		2.40	-	2.70	V
P_{tot}	total power dissipation	Operating mode		-	33	46.8	mW
		Idle mode		-	16	25.2	mW
$R_{pu(int)(RST_N)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ
I²C-bus: (5 V tolerant) pins SDA and SCL							
C_{in}	input capacitance		[3]	-	-	10	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature and V_{DD} = 3.3 V.

[2] See Section 9 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL} / I_{OH} exceeds the test condition, V_{OL} / V_{OH} may exceed the related specification.

[3] Pin capacitance is characterized but not tested.

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11. Dynamic characteristics

Table 22. Dynamic characteristics (12 MHz)

V_{DD} = 3.0 V to 3.6 V; T_{amb} = 0 °C to +70 °C for industrial applications; f_{osc} = 12 MHz (crystal); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Glitch filter						
t_{gr}	glitch rejection time	pin $\overline{RST}$	-	-	50	ns
		any pin except $\overline{RST}$	-	-	15	ns
t_{sa}	signal acceptance time	pin $\overline{RST}$	125	-	-	ns
		any pin except $\overline{RST}$	50	-	-	ns
I²C-bus: (5 V tolerant) pins SDA and SCL						
f_{clk}	clock frequency	Standard mode	-	-	100	kHz
		Fast mode	-	-	400	kHz

12. Application information

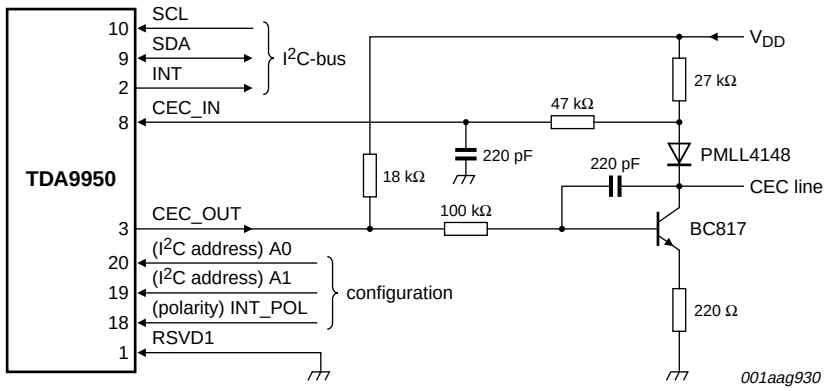
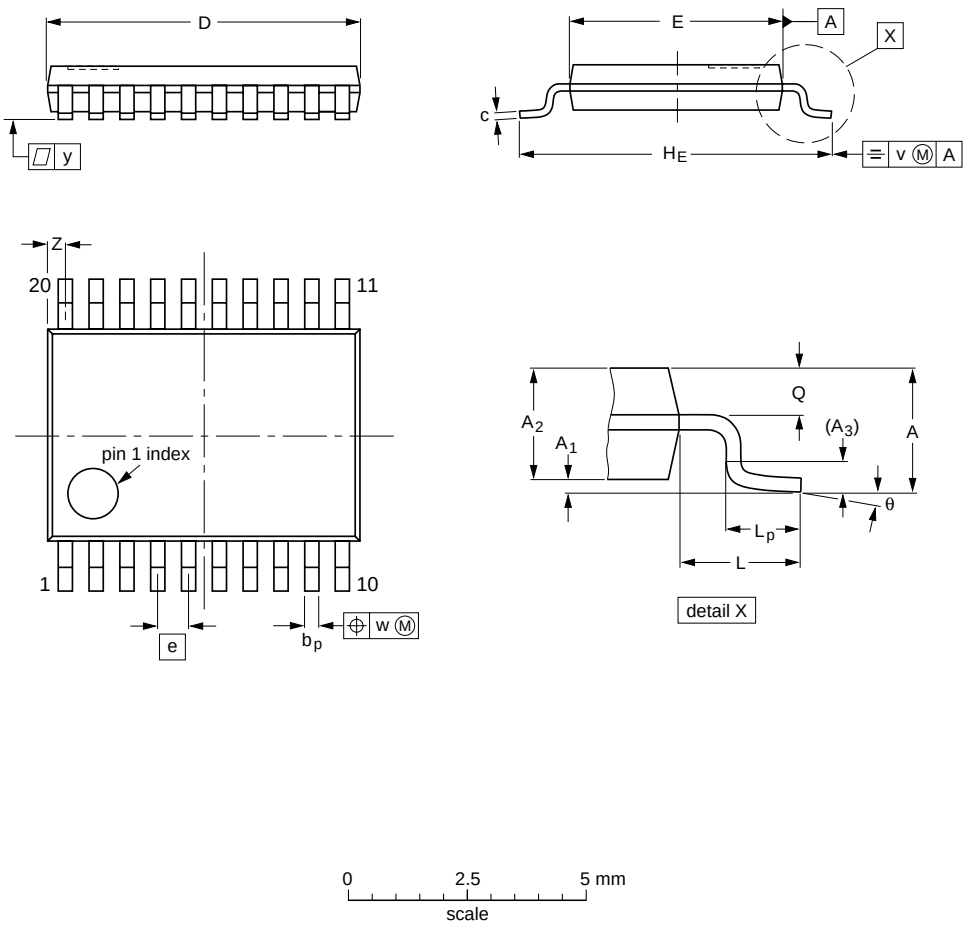


Fig 9. Application diagram

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13. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT360-1 (TSSOP20)

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14. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9950_2	20091022	Product data sheet	-	TDA9950_1
Modifications:	• Figure 1 “Block diagram”: removed pin name CEC_POL • Figure 2 “Pin configuration”: changed pin name CEC_POL by RSVD1 • Table 3 “Pin description”: changed pin name CEC_POL by RSVD1 • Table 3 “Pin description”: updated description pin CEC_OUT • Figure 9 “Application diagram”: changed pin name CEC_POL by RSVD1			
TDA9950_1	20071116	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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